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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,508	02/12/2004	Alfredo Aldereguia	RPS9 2003 0207 US1	5244

56102 7590 04/16/2008

IBM (RPS-BLF)
c/o BIGGERS & OHANIAN, LLP
P.O. BOX 1469
AUSTIN, TX 78767-1469

EXAMINER	
CHU, WUTCHUNG	

ART UNIT	PAPER NUMBER
2619	

MAIL DATE	DELIVERY MODE
04/16/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,508	ALDEREGUIA ET AL.	
	Examiner	Art Unit	
	WUTCHUNG CHU	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/12/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This communication is in response to application's amendment filed on 1/31/2008. Claims 1-21 are pending.

Claim Objections

2. Claim 7 is objected to because of the following informalities: the term "interconections" is misspelled. Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 8-10, and 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Leigh (US2003/0158940).

Regarding claim 1, Leigh discloses method for integrated load balancing among peer servers **(see paragraph 7)** comprising:

- a first set of central processing units **(see paragraph 29 CPUs)**;
- a first system memory accessible to the first set of processors **(see paragraph 29 processors)**;

- scalability logic **(see paragraph 29 scalability logic is not further specified therefore it is broadly interpreted as load balancing algorithms)** to connect the data processing system to a second data processing system, having a second set of processors and a second system memory, to form a scaled system **(see paragraph 29 and figure 1c)**;

- a set of scalability ports **(see paragraph 40the configuration shown is only one possible arrangement of connections among the ports; many other permutations are possible. Not all of the possible connection configurations are optimal for a chosen load balancing method)** connected to the scalability logic to receive scalability cables **(see paragraph 40 interconnecting cables among the ILBs)** connecting the first system to the second system **(see paragraph 29 and figure 1a-d)**; and

- system management to cause each of the system's scalability ports **(see paragraph 40the configuration shown is only one possible arrangement of connections among the ports; many other permutations are possible. Not all of the possible connection configurations are optimal for a chosen load balancing method)** to issue an identifiable signal **(see paragraph 30 request)** and further configured to detect the reception of an identifiable signal **(see paragraph 30 ILB 50 acknowledges the load shedding request from ILB 10)**, sent by another system, by any of the scalability ports **(see paragraph 40the configuration shown is only one possible arrangement of connections among the ports; many other permutations are possible. Not all of the**

possible connection configurations are optimal for a chosen load balancing method) and to report the reception of the signal to a system management of the second system to determine which ports of the two systems are connected by the cable **(see paragraph 47 and figure 1 a-d each port knows the ID of the port of ports to which it is directly connected and see paragraph 40 interconnecting cables among ILBs)**.

Regarding claim 2, Leigh teaches the system management includes a service processor connected to the system via an adapter card and wherein the service processor is connected to a service processor of other systems via a network medium **(see paragraph 49 figure 1a-d and figure 3 zone A-D ref311-4 and ref306 external network)**.

Regarding claim 8, Leigh teaches a method of determining scalability cabling between at least two scalable data processing systems, comprising:

- driving an identifiable signal on a first scalability port **(see paragraph 40the configuration shown is only one possible arrangement of connections among the ports; many other permutations are possible. Not all of the possible connection configurations are optimal for a chosen load balancing method)** of a first system **(see paragraph 30 request)**;

- responsive to receiving the identifiable signal by a second system, determining which scalability port **(see paragraph 40the configuration shown is only one possible arrangement of connections among the**

ports; many other permutations are possible. Not all of the possible connection configurations are optimal for a chosen load balancing method) of the second system received the distinctive signal **(see paragraph 30 acknowledge)**;

- informing the first system of the reception of the distinctive signal **(see paragraph 30 acknowledge)** by the determined scalability port **(see paragraph 40the configuration shown is only one possible arrangement of connections among the ports; many other permutations are possible. Not all of the possible connection configurations are optimal for a chosen load balancing method)** of the second system and recording the first scalability port **(see paragraph 40the configuration shown is only one possible arrangement of connections among the ports; many other permutations are possible. Not all of the possible connection configurations are optimal for a chosen load balancing method)** of the first system and the scalability port of the second system as being connected by a scalability cable **(see paragraph 30 ILB 0 provides ILB 10 with a list of ILBs that can accept the load and with the load-shedding conditions)**.

Regarding claim 9, Leigh teaches further comprising detecting a timeout by the first system and, responsive thereto, identifying the first scalability port **(see paragraph 40the configuration shown is only one possible arrangement of connections among the ports; many other permutations are possible. Not all of the possible connection configurations are optimal for a chosen load balancing method)** as

being unconnected **(see paragraph 47 port 24 know it is not connected and figure 1b ref24)**.

Regarding claim 10, Leigh teaches further comprising, iterating the sequence of claim 8, until all scalability ports **(see paragraph 40the configuration shown is only one possible arrangement of connections among the ports; many other permutations are possible. Not all of the possible connection configurations are optimal for a chosen load balancing method)** have been accounted for **(see paragraph 47 and figure 1a-d and paragraph 30 ILB 0 provides ILB 10 with a list of ILBs that can accept the load and with the load-shedding conditions)**.

Regarding claims 15-17, Leigh teaches programming **(see paragraph 42)** and disclose all the limitations as discussed in the rejection of claims 8-10 and are therefore claims 15-17 are rejected using the same rationales.

Claim Rejections - 35 USC § 103

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 6-7, 11-12, 14, 18-19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leigh in view of Nakamura (US2004/0057448).

Regarding claims 3 and 14, Leigh teaches

- the system management causes a scalability port **(see paragraph 40the configuration shown is only one possible arrangement of connections among the ports; many other permutations are possible. Not all of the possible connection configurations are optimal for a chosen load balancing method)** to issue an identifiable signal

disclose all the subject matter of the claimed invention with the exception of

- by causing the assertion of a bit in a register corresponding to the set of scalability ports.
- determining the scalability port that received the signal includes reading the bits in a register associated with scalability port.

Nakamura from the same or similar fields of endeavor teaches the use of the communication ports of those nodes are assigned port numbers to identify these ports, the 1394 interface of each node automatically recognizes a new connection configuration, and assignment of node Ids **(see Nakamura paragraph 122 and paragraphs 179 and 180 where node ID is being assigned and paragraph 152 communication ports of those nodes are assigned port number to identify these**

ports and paragraph 155 nodes declare parent-child relationships among their communication port, therefore when assigning node ID, ports are also assigned with their relationship to other nodes and figure 6 ref602 node ID# and figure 14, fig. 15 fig. 16), and upon receiving the self ID packet, each node can recognize the node numbers assigned to the respective nodes and can detect a node number assigned to itself **(see Nakamura paragraph 187)**. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the assigning node ID and identify communication ports as taught by Nakamura in the integrated load balancing among peer server of Leigh in order to enhance system efficiency.

Regarding claim 6, Leigh teaches identifying the corresponding scalability port **(see paragraph 40the configuration shown is only one possible arrangement of connections among the ports; many other permutations are possible. Not all of the possible connection configurations are optimal for a chosen load balancing method)** open **(see Leigh paragraph 47 and figure 1b port 24)** and disclose all the subject matter of the claimed invention with the exception of the system management includes means for determining a timeout condition following assertion of a bit.

Nakamura from the same or similar fields of endeavor teaches the use of the communication ports of those nodes are assigned port numbers to identify these ports, the 1394 interface of each node automatically recognizes a new connection configuration, and assignment of node Ids **(see Nakamura paragraph 122 and paragraph 152-162 and figure 6 ref602 node ID# and figure 14, fig. 15 fig. 16)**. Thus, it would have been obvious to one of ordinary skill in the art at the time of the

invention to use the assigning node ID and identify communication ports as taught by Nakamura in the integrated load balancing among peer server of Leigh in order to enhance system efficiency.

Regarding claim 7, Leigh disclose all the subject matter of the claimed invention with the exception of the system management further includes code means for using the scalability information to generate a graphical image of scalability interconections.

Nakamura from the same or similar fields of endeavor teaches the use of display function **(see Nakamura paragraph 236 and 237)**. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the display function as taught by Nakamura in the integrated load balancing among peer server of Leigh in order to provide enhance efficiency in system monitoring.

Regarding claims 11-12, 18-19, and 21, Leigh and Nakamura disclose all the limitations as discussed in the rejection of claims 3, 7, and 14 and are therefore claims 11-12, 18-19, and 21 are rejected using the same rationales.

6. Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Leigh and Nakamura further in view of Vegter (US.6286073).

Regarding claim 4 and 5, Leigh and Nakamura disclose all the subject matter of the claimed invention with the exception of

- the scalability port register is implemented in a programmable logic device.

- the system management further includes controller logic connected to the service processor via a dedicated serial connection and connected to the programmable logic device via an I2C bus.

Vegter from the same or similar fields of endeavor teaches the use of I2C control block may be a programmable logic array **(see Vegter col. 3 lines 21-42)**.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the programmable logic array as taught by Vegter in the modified integrated load balancing among peer server of Leigh and Nakamura in order to provide enhance efficiency in system monitoring solution for interfacing integrated circuits to one another, when it is necessary to interface an external I2C device with a personal computer, additional hardware is typically needed which is expensive, cumbersome to use and not versatile. Thus, the integrated circuit art has not heretofore created a solution for simple and effective I2C interfacing between a personal computer and any I2C device **(see Vegter col. 1 lines 46-54)**.

7. Claims 5, 13, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leigh in view of Vegter (US.6286073).

Regarding claim 5, Leigh disclose all the subject matter of the claimed invention with the exception of

- the system management further includes controller logic connected to the service processor via a dedicated serial connection and connected to the programmable logic device via an I2C bus.

Vegter from the same or similar fields of endeavor teaches the use of I2C control block may be a programmable logic array **(see Vegter col. 3 lines 21-42)**, and it is well known in the art to use the service processor via a dedicated serial connection and programmable logic device via an I2C bus.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the I2C control block may be a programmable logic array as taught by Vegter in the modified integrated load balancing among peer server of Leigh and Nakamura in order to provide enhance efficiency in system monitoring solution for interfacing integrated circuits to one another, when it is necessary to interface an external I2C device with a personal computer, additional hardware is typically needed which is expensive, cumbersome to use and not versatile. Thus, the integrated circuit art has not heretofore created a solution for simple and effective I2C interfacing between a personal computer and any I2C device **(see Vegter col. 1 lines 46-54)**.

Regarding claims 13 and 20, Leigh, Nakamura, and Vegter disclose all the limitations as discussed in the rejection of claims 5 and are therefore claims 13 and 20 are rejected using the same rationales.

Response to Arguments

8. Applicant's arguments, see applicant's remarks on Page 7, filed 1/31/2008, with respect to objections to the Drawings have been fully considered and are persuasive. The objections of drawings of figures 2 and 3 have been withdrawn.

9. Applicant's arguments filed 1/31/2008 on page 8 regarding claim objection of a typo in claim 7 – "interconection". The have been fully considered but they are not persuasive. The term can not be found in dictionary and therefore objection remains and upon allowance the office reserves the right to correct the term with correct spelling.

10. Applicant's arguments, see applicant's remarks on Page 8, filed 1/31/2008, with respect to objection claim 18 have been fully considered and are persuasive. The objection of claim 18 has been withdrawn.

11. Applicant's arguments filed 1/31/2008 have been fully considered but they are not persuasive.

With regard to applicant's remark for claim 1 (page 10-12), applicant submits that Leigh does not disclose scalability logic to connect the data processing system to a second data processing system, having a second set of processors and a second system memory, to from a scaled system.

The term scalability logic is not further defined in the claim, and although the claims are interpreted in light of specification, limitations from the specification are not read into the claims. See *In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993)*. And the term therefore interpreted broadly as any scaling logic, and in this case the cited prior art's load balancing algorithm corresponds to the limitation, and therefore rejection respectfully remains.

With regard to applicant's remark for claims 1 and 8 (page 13-18), applicant submits that Leigh does not disclose a set of scalability ports connected to the

scalability logic to receive scalability cables connecting the first system to the second system.

Leigh disclose cables interconnection with ILBs in paragraph 40. Leigh also disclose load balancing algorithm, which corresponds to scalability logic, and where this logic is used among port for load balancing, therefore meeting the limitations and rejection respectfully remains.

Examiner's Note: examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the figures may apply as specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Abraham et al. (5530842)

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WUTCHUNG CHU whose telephone number is (571)270-1411. The examiner can normally be reached on Monday - Friday 1000 - 1500EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on 571 272 7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/WC/
Wutchung Chu

/Edan Orgad/
Supervisory Patent Examiner, Art Unit 2619